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10/602,292	06/24/2003	Michael B. Doerr	5860-00101	1233

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EXAMINER
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LAI, VINCENT

ART UNIT	PAPER NUMBER
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2181

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/602,292	<b>Applicant(s)</b> DOERR ET AL.	
	<b>Examiner</b> Vincent Lai	<b>Art Unit</b> 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 September 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-64 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 41-51 is/are allowed.
- 6) ☒ Claim(s) 1-26,33-40 and 52-64 is/are rejected.
- 7) ☒ Claim(s) 27-32 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All    b) ☐ Some    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. Acknowledgment is made of the amendments to the claims submitted 17 April 2006.

### ***Priority***

2. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

### ***Information Disclosure Statement***

3. The information disclosure statement (IDS) submitted on 6/10/2004 was considered by the examiner.

### ***Specification***

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Processing System with Interspersed Stall Propagating Processors and Communication Elements".

***Response to Arguments***

5. Applicant's arguments filed 5 September 2006 have been fully considered but they are not entirely persuasive.

In the pre-appeal brief, Examiner has identified three main arguments:

Applicant argues, "Contrary to the Examiner's assertion, Wilkinson fails to teach or suggest all of the limitations of claim 1, including a plurality of dynamically configurable communication elements and a plurality of dynamically configurable communication elements, each having specifically recited features, coupled together in an interspersed arrangement."

Specifically Applicant argues that the Wilkinson teaches a **uniform** array of pickets (which is the term used for the arrangement of circuitry in the reference), whereas the invention of the application is an **interspersed** arrangement of circuitry.

Wilkinson is silent on uniformity and Applicant relies on figures to prove uniformity. In the Final rejection, Examiner has noted that figures in the Application also appear uniform and expressed his definition of interspersed as being "to place at intervals." Applicant refutes this interpretation and has no further definition within the Specification to argue.

Applicant argues, "Applicants further note that claim 1 does not merely recite communication elements, but rather communication elements distinct from and coupled together with processing elements in an interspersed arrangement."

It is of note that the Applicant on page 3 of the Pre-appeal brief says that Wilkinson does disclose, "those elements are interconnected." Interconnection is not a limitation of claim 1. What is claimed is a coupling of communication elements. Coupling elements can be done as simply as connecting two elements together. Cited in the final action are column 23, lines 1-5, which disclose that data is shared among the pickets.

Applicant further argues that there is no "disclosure of how those ports are configured for coupling to subsets of both the recited processors and other ones of the recited communication elements as recited in claim 1."

As cited in the final office action, column 22, lines 30-56 and column 23, lines 1-5 detail that communication is done through I/O that is also connected to memory and that communication between pickets is down through a backplane. From the figures, it can be seen that communication between pickets involves sharing memory and thus the I/O ports are communication elements. Without the I/O ports, there is no sharing of data as each picket is an individual card.

The third argument was based on propagation of stalls. The final rejection mailed on 2 June 2006 was withdrawn and prosecution was reopened for the arguments pertaining to the propagation of stalls.

Such propagation of stalls is now deemed to be allowable subject matter. See below "Allowable Subject Matter" section.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-26, 33-40, and 52-64 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilkinson et al (U.S. Patent # 5,805,915).

As per **claim 1**, Wilkinson et al discloses a system, comprising:

a plurality of processors (Column 13, lines 38-41), each comprising at least one arithmetic logic unit (Column 15, lines 31-34), an instruction processing unit (Column 14, lines 35-38), and a plurality of processor ports (Column 22, lines 30-56); and

a plurality of dynamically configurable communication elements (Column 23, lines 11-16: DCC elements are part of the picket array), each comprising a plurality of communication ports (Column 22, lines 30-56), a first memory (Column 22, lines 63-67), and a routing engine (Column 6, lines 31-42: Part of the picket array);

wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement (Column 23, lines 11-16: Interspersed arrangement is the picket array);

wherein, for each of said processors, said plurality of processor ports are configured for coupling to a first subset of said plurality of dynamically configurable communication elements (Column 22, lines 30-56, and column 23, lines 1-5, and 11-16: The I/O ports are connected to the picket array);

wherein, for each of said dynamically configurable communication elements, said plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of said plurality of said processors and a second subset of communication ports configured for coupling to a second subset of said plurality of dynamically configurable communication elements (Column 23, lines 1-5).

As per **claim 2**, Wilkinson et al discloses wherein each of said processors is coupled to each of a plurality of neighboring dynamically configurable communication elements via a respective one of said plurality of processor ports (Column 23, lines 1-5);

wherein each of said dynamically configurable communication elements is coupled to a plurality of neighboring processors via a respective one of said first subset of said plurality of communication ports (Figure 2, element 103 & Column 23, lines 1-5);

wherein each of said dynamically configurable communication elements is coupled to each of a plurality of neighboring dynamically configurable communication

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elements via a respective one of said second subset of said plurality of communication ports (Figure 2, the left + right propagate bus & Column 23, lines 1-5).

As per **claim 3**, Wilkinson et al discloses wherein each of said processors is coupled to each of four neighboring dynamically configurable communication elements via a respective one of said plurality of processor ports (Figure 4, and Column 23, lines 1-5: Figure 4 shows that there can be as many picket arrays as one chooses; i.e. N can equal 4);

wherein each of said dynamically configurable communication elements is coupled to each of four neighboring processors via a respective one of said first subset of said plurality of communication ports (Figure 2, element 103; figure 4; and Column 23, lines 1-5);

wherein each of said dynamically configurable communication elements is coupled to each of four neighboring dynamically configurable communication elements via a respective one of said second subset of said plurality of communication ports (Figure 2, the left + right propagate bus; figure 4; and Column 23, lines 1-5).

As per **claim 4**, Wilkinson et al discloses wherein said plurality of processors and said plurality of dynamically configurable communication elements are interspersed in a substantially homogeneous fashion (Figure 2, and figure 4: To connect a picket to an array, there is no need to add additional ports or elements to a picket and thus the ratio will always be the same).



As per **claim 5**, Wilkinson et al discloses wherein, for each of said processors, said instruction processing unit is coupled to control said at least one arithmetic logic unit (Figure 2, element 101, and column 15, line 65- column 16, line 2);

wherein each of said processors further comprises at least a second memory including a plurality of addressable locations, wherein said second memory is coupled to said at least one instruction processing unit (Figure 2, elements 105 and 106, and column 19, lines 50-55); and

wherein, for each of said processors, said plurality of processor ports comprise a first subset of processor ports coupled to said at least one arithmetic logic unit (Figure 2, the left + right propagate bus & Column 23, lines 1-5) and a second subset of processor ports coupled to said instruction processing unit (Figure 2, the broadcast data/address bus & Column 23, lines 1-5).

As per **claim 6**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, said first memory is shared among a plurality of said processors (Column 15, lines 5-7).

As per **claim 7**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, said first memory is shared among a plurality of neighboring processors (Column 15, lines 5-7).

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As per **claim 8**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, said first memory is shared among four neighboring processors (Column 15, lines 5-7).

As per **claim 9**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, said first memory operates as at least a portion of a register file for its neighboring processors (Column 15, lines 34-37).

As per **claim 10**, Wilkinson et al discloses wherein each of said processors is dynamically configurable to obtain data from the first memory of different ones of said dynamically configurable communication elements (Column 18, lines 7-13).

As per **claim 11**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, said first memory stores data that is directly accessible by a processor during execution of instructions (Column 18, lines 7-13).

As per **claim 12**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, said first memory stores data that is directly accessible by each of a plurality of neighboring processors during execution of instructions (Column 15, lines 5-7).

As per **claim 13**, Wilkinson et al discloses wherein each of the processors is operable to obtain data from a first memory of any of a plurality of neighboring dynamically configurable communication elements (Column 18, lines 15-18: Done with broadcasts).

As per **claim 14**, Wilkinson et al discloses wherein a first processor is operable to obtain first data from a first memory of a first dynamically configurable communication element during a first time period, and wherein the first processor is operable to obtain second data from a first memory of a second dynamically configurable communication element during a second time period (Column 18, lines 7-18).

As per **claim 15**, Wilkinson et al discloses wherein a first processor is operable to obtain a plurality of data values from a respective subset of said plurality of dynamically configurable communication elements substantially simultaneously (Column 18, lines 7-18).

As per **claim 16**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, said first memory is configured to provide a plurality of data values to a respective subset of said plurality of processors substantially simultaneously (Column 18, lines 7-18).

As per **claim 17**, Wilkinson et al discloses wherein, for each of said dynamically configurable communication elements, the first memory is coupled to said plurality of communication ports via a plurality of access ports and includes a plurality of addressable locations (Column 18, lines 7-18); and

wherein, for each of said dynamically configurable communication elements, said routing engine is coupled to said plurality of communication ports and configured to route data between any of said plurality of communication ports (Column 15, lines 5-7).

As per **claim 18**, Wilkinson et al discloses wherein each of said plurality of dynamically configurable communication elements further comprises a direct memory access engine coupled to said plurality of communication ports and configured to transfer data between the first memory and said plurality of communication ports (Column 15, lines 5-7 and column 18, lines 7-18).

As per **claim 19**, Wilkinson et al discloses wherein different pathways are operable to be created for data transfer among different subsets of said dynamically configurable communication elements (Column 18, lines 7-18: Different select lines can created different pathways);

As per **claim 20**, Wilkinson et al discloses wherein each of at least a subset of the processors is operable to dynamically create different pathways for data transfer

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among different subsets of said dynamically configurable communication elements  
(Column 22, line 63- column 23, line 5: All elements are already connected).

As per **claim 21**, Wilkinson et al discloses wherein each of at least a subset of the dynamically configurable communication elements is operable to dynamically create pathways among different subsets of said dynamically configurable communication elements (Column 22, line 63- column 23, line 5).

As per **claim 22**, Wilkinson et al discloses wherein a first pathway comprises a first plurality of dynamically configurable communication elements; wherein, for each of the first plurality of dynamically configurable communication elements in the first pathway, the first pathway is dynamically created by configuring the routing engine of the dynamically configurable communication element to implement a portion of the first pathway prior to initiating a data transfer (Column 22, line 63- column 23, line 5).

As per **claim 23**, Wilkinson et al discloses wherein a given pathway is dynamically created via, for each of said subset of said dynamically configurable communication elements, configuring said routing engine to implement said pathway in response to receiving a first portion of a data transfer, wherein said first portion includes routing information (Column 22, line 63- column 23, line 5).

As per **claim 24**, Wilkinson et al discloses wherein each pathway is operable to be destroyed, wherein a given pathway remains available for data transfer until destroyed (Column 22, line 63- column 23, line 5).

As per **claim 25**, Wilkinson et al discloses wherein a respective pathway is operable to remain available regardless of any transfer of message data on the respective pathway (Column 22, line 63- column 23, line 5).

As per **claim 26**, Wilkinson et al discloses wherein a first processor is operable to configure a first dynamically configurable communication element to provide data directly to a neighboring second dynamically configurable communication element (Column 23, lines 1-5);

wherein the first processor is operable to create a pathway between the first dynamically configurable communication element and a remote third dynamically configurable communication element to enable the first dynamically configurable communication element to provide data through the pathway to the remote third dynamically configurable communication element (Column 23, lines 1-5).

As per **claim 33**, Wilkinson et al discloses wherein one of said processors is configurable as a source device to transfer a first plurality of data through an intermediate subset of said plurality of dynamically configurable communication elements to a destination device (Column 23, lines 1-5);

wherein, after said source device begins transfer of said first plurality of data through said intermediate subset to said destination device, if one of said source device, one of said intermediate subset, or said destination device stalls, the stalling device is operable to propagate stalling information through one or more of said intermediate subset to one or more of said source device and said destination device (Column 19, lines 10-20);

wherein said source device is operable to suspend transfer of said first plurality of data upon receipt of said stalling information, wherein a portion of said first plurality of data transmitted after said stalling and prior to the suspending is buffered in at least one of said intermediate subset (Column 19, lines 10-20);

wherein said destination device is operable to suspend processing of said first plurality of data upon receipt of said stalling information (Column 19, lines 10-20).

As per **claim 34**, Wilkinson et al discloses wherein, if said stalling device becomes available for communication, said stalling device is operable to propagate communication availability information through one or more of said intermediate subset to one or more of said source device and said destination device (Column 19, lines 10-20);

wherein said at least one of said intermediate subset transmits said portion of said first plurality of data to said destination device after said stalling device becomes available for communication (Column 19, lines 10-20);

wherein said source device resumes transfer of said first plurality of data upon receipt of said communication availability information (Column 19, lines 10-20);

wherein said destination device resumes processing of said first plurality of data upon receipt of said communication availability information (Column 19, lines 10-20).

As per **claim 35**, Wilkinson et al discloses wherein said first plurality of data is conveyed via a plurality of data signals (Column 19, lines 10-20);

wherein said stalling information is conveyed via a blocked signal and an idle signal (Column 19, lines 10-20);

wherein said blocked signal and said idle signal are routed parallel to said plurality of data signals (Column 19, lines 10-20).

As per **claim 36**, Wilkinson et al discloses wherein each of said dynamically configurable communication elements further comprises:

a plurality of input ports (Column 22, lines 30-58);

a plurality of output registers (Figure 2, elements 105 and 106, and column 19, lines 50-55);

a crossbar coupled to receive data from one or more of said plurality of input ports and to transmit data to a selected one or more of said plurality of output registers (Column 23, lines 1-5);

wherein each said output register selectively operates in a synchronous data transfer mode or a transparent data transfer mode (Column 8, line 64- column 9, line 6).



As per **claim 37**, Wilkinson et al discloses wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit (Column 18, line 56: The check for VLSI rules indicates that chip is manufactured on an integrated circuit).

As per **claim 38**, Wilkinson et al discloses wherein each of at least a subset of the processors is operable to be enabled/disabled as needed to reduce power consumption (Column 17, lines 59-64).

As per **claim 39**, Wilkinson et al discloses wherein each of at least a subset of the processors is operable to operate in a synchronous fashion (Column 8, line 64-column 9, line 6).

As per **claim 40**, Wilkinson et al discloses wherein the first memory (Figure 2, element 102) of each of the dynamically configurable communication elements (Figure 2, element 100) comprises only an accumulator (Figure 2, element 101), a status register (Figure 2, element 105 & 106), operand buffers (Figure 2, element 104), and one or more address generator controls (Figure 2, elements 107).

As per **claim 52**, Wilkinson et al discloses a system, comprising:

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a plurality of processors (Column 13, lines 38-41), each comprising at least one arithmetic logic unit (Column 15, lines 31-34), at least one instruction processing unit (Column 14, lines 35-38), and a plurality of processor ports (Column 22, lines 30-56);

a plurality of dynamically configurable communication elements (Column 23, lines 11-16), each comprising a plurality of communication ports (Column 22, lines 30-56), at least a first memory (Column 22, lines 63-67), and a routing engine (Column 6, lines 31-42);

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit (Column 18, line 56);

wherein the plurality of processors and the plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement (Column 23, lines 11-16);

wherein each of said dynamically configurable communication elements comprises:

a plurality of input ports (Column 22, lines 30-58);

a plurality of output registers (Figure 2, elements 105 and 106, and column 19, lines 50-55);

a crossbar coupled to receive data from one or more of said plurality of input ports and to transmit data to a selected one or more of said plurality of output registers (Column 23, lines 1-5);

wherein each said output register selectively operates in a synchronous data transfer mode or a transparent data transfer mode (Column 8, line 64- column 9, line 6).

As per **claim 53**, Wilkinson et al discloses wherein, for each of said processors, said at least one instruction processing unit is coupled to control said at least one arithmetic logic unit (Column 15, lines 31-34);

wherein each of said processors further comprises at least a second memory including a plurality of addressable locations (Figure 2, elements 105 and 106, and column 19, lines 50-55),

wherein said second memory is coupled to said at least one instruction processing unit (Figure 2); and

wherein the plurality of processor ports comprise a first subset of processor ports coupled to said at least one arithmetic logic unit (Figure, the left + right propagate bus and column 23, lines 1-5) and a second subset of processor ports coupled to said at least one instruction processing unit (Figure 2, the broadcast data/address bus and column 23, lines 1-5).

As per **claim 54**, Wilkinson et al discloses wherein said plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of said plurality of processors and a second subset of communication ports configured for coupling to a subset of said plurality of dynamically configurable communication elements (Column 23, lines 1-5);

wherein said at least a first memory is coupled to said plurality of communication ports via a plurality of access ports and includes a plurality of addressable locations (Column 15, lines 5-7); and

wherein said routing engine is coupled to said plurality of communication ports and configured to route data between any of said plurality of communication ports (Column 15, lines 5-7).

As per **claim 55**, Wilkinson et al discloses wherein each of said plurality of dynamically configurable communication elements further comprises a direct memory access engine coupled to said plurality of communication ports and configured to transfer data between said at least a first memory and said plurality of communication ports (Column 15, lines 5-7 and column 18, lines 7-18).

As per **claim 56**, Wilkinson et al discloses a system, comprising:  
an interconnect network (Column 6, lines 31-42: The picket array is an interconnect network); and  
a plurality of dynamically configurable communication elements configured to exchange data, each said element comprising:

a plurality of input ports coupled to said interconnect network (Column 22, lines 30-58);

a plurality of output registers coupled to said interconnect network (Figure 2, elements 105 and 106, and column 19, lines 50-55);

a crossbar coupled to receive data from one or more of said plurality of input ports and to transmit data to a selected one or more of said plurality of output registers (Column 23, lines 1-5);

wherein each said output register selectively operates in a synchronous data transfer mode or a transparent data transfer mode (Column 8, line 64-column 9, line 6).

As per **claim 57**, Wilkinson et al discloses a method for transferring data from a source device to a destination device, wherein said source device is coupled to said destination device through a plurality of intermediate devices, the method comprising:

configuring said source device to transfer a first plurality of data to said destination device through said plurality of intermediate devices (Column 19, lines 10-20);

configuring each of said plurality of intermediate devices to operate in a synchronous data transfer mode or a transparent data transfer mode (Column 19, lines 10-20);

transferring said first plurality of data through a single intermediate device during a single master clock cycle dependent upon said single intermediate device being configured to operate in a synchronous data transfer mode (Column 19, lines 10-20);  
and

transferring said first plurality of data through multiple intermediate devices during a single master clock cycle dependent upon each of said multiple intermediate

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devices being configured to operate in a transparent data transfer mode (Column 19, lines 10-20).

As per **claim 58**, Wilkinson et al discloses wherein the method operates in a system comprising a plurality of processors (Column 13, lines 38-41) and a plurality of dynamically configurable communication elements (Column 23, lines 11-16);

wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement (Column 23, lines 11-16);

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit (Column 18, line 56).

As per **claim 59**, Wilkinson et al discloses wherein said source device comprises one of said processors (Figure 2 and column 13, lines 38-41);

wherein said plurality of intermediate devices comprise a plurality of dynamically configurable communication elements (Column 23, lines 11-16);

As per **claim 60**, Wilkinson et al discloses wherein each of said plurality of processors comprises at least one arithmetic logic unit (Column 15, lines 31-34), at least one instruction processing unit (Column 14, lines 35-38), and a plurality of processor ports (Column 22, lines 30-56);

wherein each of said plurality of dynamically configurable communication elements comprises a plurality of communication ports (Column 22, lines 30-56), at least one memory (Column 22, lines 63-67), and a routing engine (Column 6, lines 31-42).

As per **claim 61**, Wilkinson et al discloses a method for transferring data from a source device to a plurality of destination devices, wherein said source device is coupled to each of said destination devices through a plurality of intermediate devices, the method comprising:

configuring said source device to transfer a first plurality of data to a first destination device through one or more intermediate devices (Column 19, lines 10-20);

configuring each of said plurality of intermediate devices to operate in a synchronous data transfer mode (Column 8, line 64- column 9, line 6);

transferring said first plurality of data from said source device to said first destination device during a first time period, wherein said first time period comprises one or more master clock cycles, and wherein said transferring comprises transferring the first plurality of data through a single intermediate device during each said master clock cycle (Column 19, lines 10-20);

configuring said source device to transfer a second plurality of data to a second destination device through said plurality of intermediate devices (Column 19, lines 10-20);

configuring each of said plurality of intermediate devices to operate in a transparent data transfer mode (Column 8, line 64- column 9, line 6);

transferring said second plurality of data from said source device to said second destination device through multiple intermediate devices during a single master clock cycle devices (Column 19, lines 10-20).

As per **claim 62**, Wilkinson et al discloses a method of manufacturing an integrated circuit, the method comprising:

fabricating a unit comprising a processor and a dynamically configurable communication element (Column 13, lines 38-41 and column 23, lines 11-16);

wherein the processor comprises an arithmetic logic unit (Column 15, lines 31-34), an instruction processing unit (Column 14, lines 35-38), and a plurality of processor ports (Column 22, lines 30-56);

wherein the dynamically configurable communication element comprises a plurality of communication ports (Column 22, lines 30-56), a first memory (Column 22, lines 63-67), and a routing engine (Column 6, lines 31-42);

placing and interconnecting a plurality of said units on a substrate, wherein said plurality of processors and said plurality of dynamically configurable communication elements are coupled together in an interspersed arrangement (Column 23, lines 11-16);



wherein, for each of said processors, said plurality of processor ports are configured for coupling to a first subset of said plurality of dynamically configurable communication elements (Column 22, lines 30-56, and column 23, line 1-5 and 11-16);

wherein, for each of said dynamically configurable communication elements, said plurality of communication ports comprise a first subset of communication ports configured for coupling to a subset of said plurality of processors and a second subset of communication ports configured for coupling to a second subset of said plurality of dynamically configurable communication elements (Column 23, lines 1-5).

As per **claim 63**, Wilkinson et al discloses a system, comprising:

a plurality of processors, each comprising:

at least one arithmetic logic unit (Column 15, lines 31-34);

at least one instruction processing unit coupled to control said arithmetic logic unit (Figure 2, element 101) and including at least a first memory (Figure 2, element 102) including a plurality of addressable locations (Figure 2, element 102); and

a plurality of processor ports, including a first subset coupled to said arithmetic logic unit (Figure 2, the left + right propagate bus and column 23, lines 1-5) and a second subset coupled to said instruction processing unit (Figure 2, the broadcast/data address bus and column 23, lines 1-5); a plurality of dynamically configurable communication elements, each comprising:

a plurality of communication ports, including a third subset configured for coupling to a subset of said plurality of processors and a fourth subset configured for coupling to a subset of said plurality of dynamically configurable communication elements (Column 22, lines 30-56);

at least a second memory coupled to said plurality of communication ports via a plurality of access ports and including a plurality of addressable locations;

a routing engine coupled to said plurality of communication ports and configured to route data between any of said plurality of communication ports (Column 15, lines 5-7); and

a direct memory access engine coupled to said plurality of communication ports and configured to transfer data between said second memory and said plurality of communication ports (Column 15, lines 5-7 and column 18, lines 7-18);

wherein said plurality of processors and said plurality of dynamically configurable communication elements are manufactured on a single integrated circuit (column 18, line 56).

As per **claim 64**, Wilkinson discloses wherein for at least one of said dynamically configurable communication elements, said first memory includes a plurality of addressable locations and is configured to substantially simultaneously provide a plurality of values stored in said plurality of addressable locations to two or more of said processors (See column 23, lines 1-5 and explanation below).

***Allowable Subject Matter***

7. Claims 41-51 are allowed.

The primary reasons for allowance of claims 41, 43, 45, and 49 are in the instant application rest at least in the combination with the inclusion of the limitation that "a stalling processor of DCC element is operable to propagate stalling information through one or more of intermediate subset of DCC elements to a source processor that is operable to suspend transfer of the first plurality of data upon receipt of the stalling information." The prior art of record neither anticipates nor renders obvious the above-recited combination.

Because claims 42, 44, 46-48, 50, and 51 depend directly or indirectly on any of the claims 41, 43, 45, and 49, these claims are considered allowable for at least the same reasons noted above with respect to claims 41, 43, 45, and 49.

8. Claims 27-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 27 and 30 have similar limitations to claims 41, 43, 45, and 49 and would be allowable for similar reasons.

Because claims 28, 29, 31, and 32 depend directly or indirectly on any of the claims 27 and 30, these claims are considered allowable for at least the same reasons noted above with respect to claims 27 and 30.

[Examiner's Note: In light of the reasons for allowable subject matter, a similar objection of the title in respect to a previous withdrawn objection is herein submitted. Given the primary reasons for allowance is due to stall propagation, Examiner now regards the new suggested title would be an improved designation for the invention]

### ***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Vincent Lai  
Examiner  
Art Unit 2181

vi  
March 1, 2007



DONALD SPARKS  
SUPERVISORY PATENT EXAMINER